Parasitic Challenges and Solutions with the Quantus QRC Extraction Solution for 7nm FinFET Designs

Cadence Design Systems

ABSTRACT

As process technology scaling reaches the realm of 10/7nmnm and below regimes, the challenges facing the foundry and design community are multi-faceted. The benefits of scaling have to be achieved with holistic process and design optimizations such that chip performance can still be improved per Moore's law, notwithstanding the physics effects, lithography effects (minus EUV) and other process effects at such atom level physical dimensions.

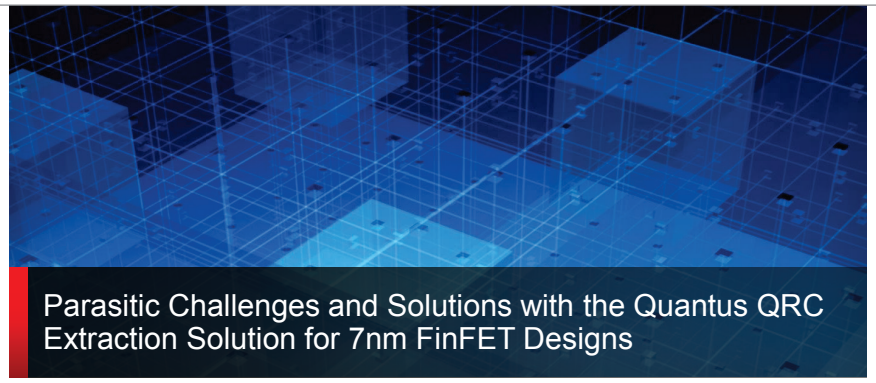
In this paper, the challenges of quasi-3D MEOL parasitic capacitance modeling, 10/7nmnm specific color mask modeling for lithography effects, as well as high performance blocking modeling are outlined and the subsequent validations and application of these modeling and extraction technologies for 10nm process development and designs are presented.

The most challenging aspect of MEOL parasitic modeling and model-based capacitance extraction is the introduction of 3D FinFET transistors which leads to severe 3D fringing cap distributions around MOS devices. In the 10/7nmnm 3D FinFET process node, the 3D MEOL modeling challenges are compounded by the unique 3D layouts which are necessary for process and design and optimizations. Quantus's unique quasi-3D modeling technology enabled the most silicon accurate extractions of FinFET-based designs such as standard cells, SRAM and PLL/VCO, which are the foundation of process development for 10/7nmnm process node.

For BEOL development, the impacts of HPB, with the intention of improving design performances, need to be accurately modeled by parasitic capacitance extractors such that large SOC designs with the aforementioned special process feature are possible. With EUV technology still absent from 10/7nm node, the needs for multiple patterning process steps mandate the development of new color aware mask modeling and extraction technologies in order to enable the shortest path of design to silicon.

SRAM design spans both MEOL and BEOL. It is a key part in the development of new process nodes in terms of process optimizations for best IP performance and lowest power consumptions. Consequently, It is essential that SRAM extractions have very tight capacitance accuracy, perfect bit-line match, as well as very good reduction accuracy, manageable simulation runtime for timing, EM/IR flow with large macros. Hence, there is a need for massively parallel field solver (3D) capability which is required to extract accurately without elongating extraction runtimes.

From designer's point of view, a tightly integrated extraction capabilities in implementation is a MUST at these FinFET nodes. In addition to the challenges presented for these nodes, we will also discuss the accuracy discuss the accuracy correlation with 3D field solver and performance of the extraction tool in addition to overall convergence and productivity benefits of the flow at 16nm and below nodes including 7nm.



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TSMC OIP Ecosystem Forum
San Jose, California
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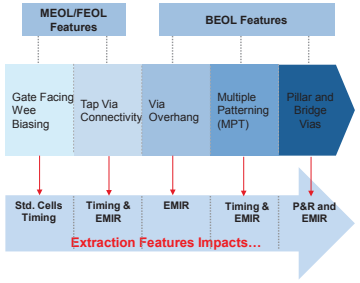
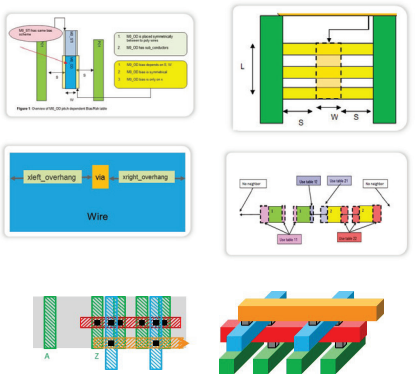
7nm Parasitic Extraction Challenges and Requirements





Full digital flow decision can't be minimized at 7nm. Imperative to make full flow commitment!

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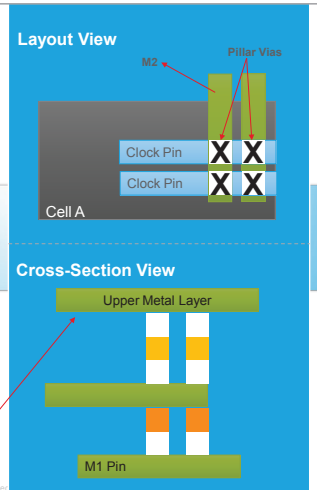
Pillar Via

Non-standard via structures (typically used on signal wires)

Employed to allow more layout compaction and less resistive paths across the chip

Placement and routing:
- May be placed at closer spacing distances than single cut via
- May also be routed through many metal layers up the stack to take CLK nets to upper-level routing layers



Parasitics Impact

STA

Cadence® Quantus™ QRC Extraction Solution will extract simplified network for accurate STA analysis

EMIR

Quantus QRC Extraction Solution extracts a more accurate resistor network for accurate EMIR analysis

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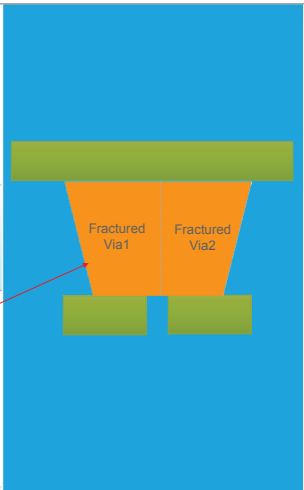
Bridge Via

More robust connectivity (typically used for power/ground nets); allows multiple routes on the same layer to be connected

Via (orange) is fractured into 2

Each via resistor is netlisted separately, connecting its upper metal portion to its lower metal portion



Parasitic Impact

EMIR

EM must be checked based on total area rather than individual via resistor

STA

EMIR

Quantus QRC Extraction Solution accurately extracts the vias for STA and EMIR analysis

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Cadence + TSMC Deliver Signoff-Extraction Solution

Engage
Collaboration on 7nm modeling features requirements between Quantus R&D and TSMC requirements for an extraction tool

Enable
Implement in Quantus and Quantus Field Solver, validate versus TSMC baseline, and enable PDK ready for mutual customers

Empower
Certification and PDK delivery to foundry customers

Mutual Customer Success!

Key Challenges: Parasitic Extraction and Design Flow

1 2 3 4 5

ACCURACY
Introduction of new modeling features including MPT requires complex modeling to provide better **accuracy**

NETLIST SIZE
Explosion in parasitics results in bigger **netlist impacting post-layout simulation** performance

DESIGN CLOSURE
Lack of correlation with **in-design** and signoff extraction; and integration in implementation platforms impact **convergence and loss of productivity**

ECO OPTIMIZATION
Signoff quality extraction is required during timing ECO optimization to reduce number of iterations to meet tape out schedule

ACCURATE EMIR
Integrated EMIR solution is a MUST to tackle **accuracy** of complex EM rule checks required for FinFET designs

Quantus Extraction Overview

Accuracy
- Foundry certified for all nodes
- Best accuracy vs foundry golden
- Color-aware (DPT/MPT/SADP)

Performance
- Massively parallel—100s of CPUs
- Fastest single and multi-corner extraction
- 3X smaller netlist for faster simulation runtimes

Integration
- Cadence Innovus™ Implementation System for digital extraction
- Cadence Virtuoso® custom design platform for transistor extraction
- Cadence Tempus™ Timing Signoff Solution, Voltus™, Voltus-Fi, and Physical Verification System (PVS) solutions

Automotive
- PowerMos flow in Virtuoso custom design platform
- Accurate Rdson
- Integrated with Voltus-Fi and Spectre® for simulation/visual

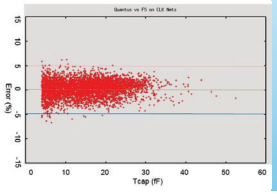
Market-Leading Features
- Inductance extraction for LEF/DEF & GDS
- Substrate Noise Analysis (SNA)

3D Field Solver
- Random-walk based solver
- Faster and accurate for characterization of standard Cells, Memory, IP, and Automotive designs

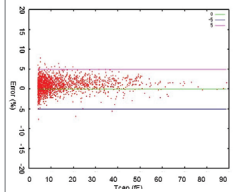
The Quantus QRC Extraction Solution is **industry's most trusted** parasitic extraction tool used by leading foundries in production for advanced nodes 10nm and below.

Accurate RCs for All Advanced-Node Designs

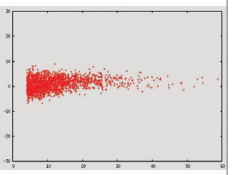
01
7nm: vs Quantus FS
CLK Nets
Mean = 0.31%
Stdev = 1.67%

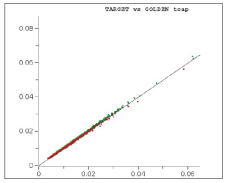


02
7nm: vs Quantus FS
Signal Nets
Mean = 0.98%
Stdev = 2.18%



03
7nm: vs Quantus FS
3000 Random Nets
Mean = 1.02%
Stdev = 2.47%

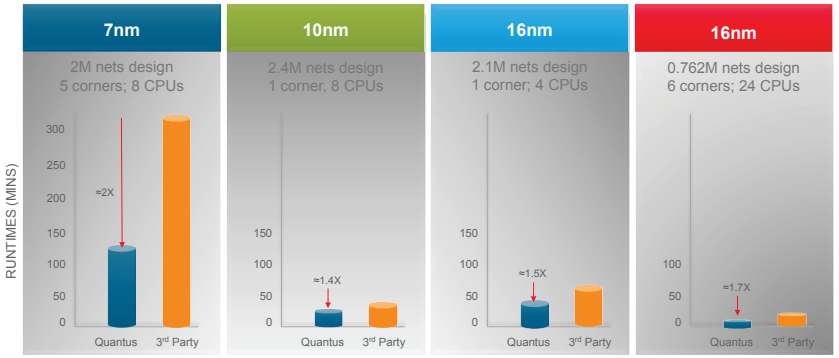




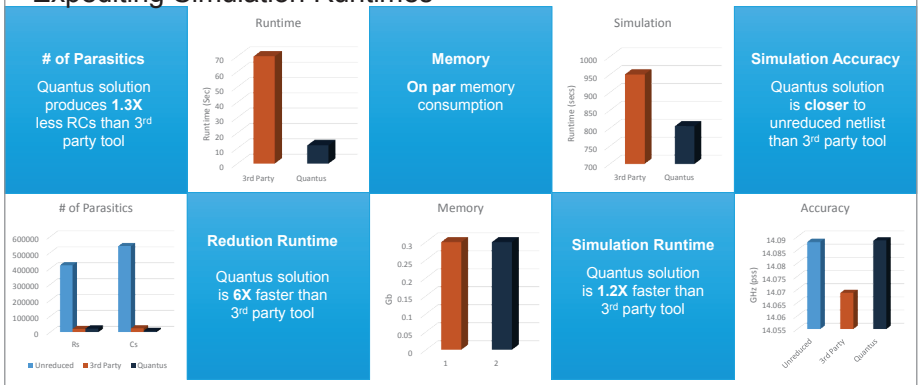
04
7nm: vs Quantus FS
2500 Random Nets
Mean = 1.06%
Stdev = 2.35%

Faster Extraction Tool in the Market for FinFET Designs

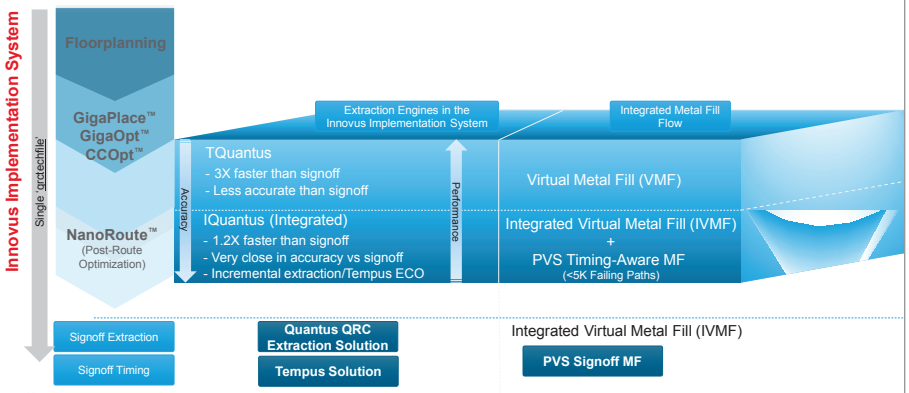
Quantus QRC Extraction Solution is ≈1.6X faster for all FinFET designs



Quantus QRC Extraction Solution Produces Smallest Netlist Expediting Simulation Runtimes

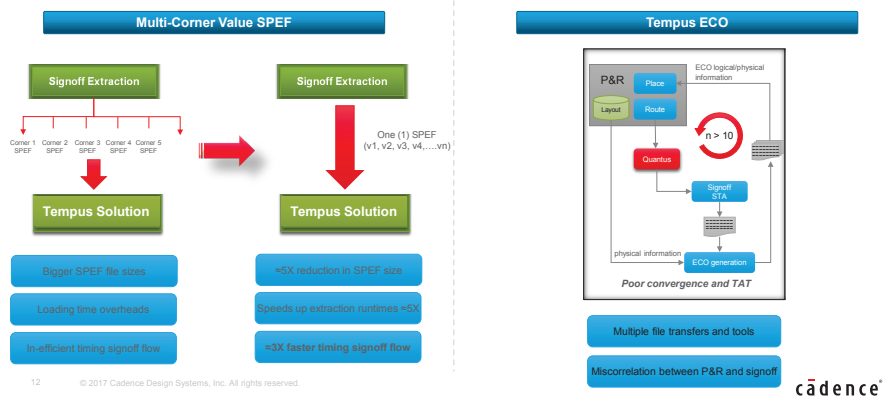


Innovus Implementation System and Quantus Signoff Extraction Solution: Three Engines in One

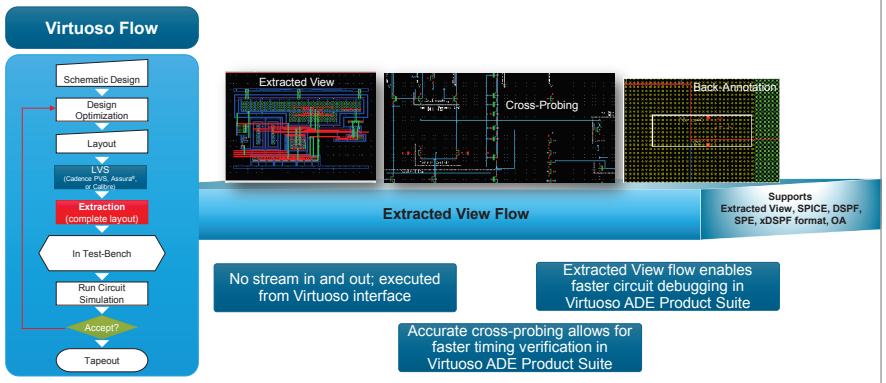


Quantus QRC Extraction Solution + Tempus Timing Signoff Solution

Most accurate and fastest timing signoff flow



Virtuoso Custom Design Platform + Quantus QRC Extraction Solution



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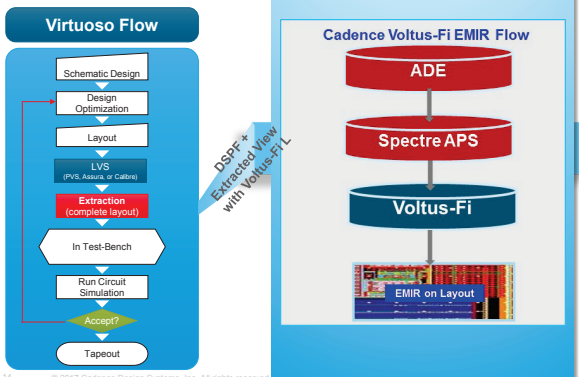
Quantus and Voltus-Fi for Accurate EMIR for FinFET Designs

EM and IR Techfile QAed with Voltus and Voltus-Fi by using Quantus QRC Extraction Solution



- Comprehensive solution in an integrated Virtuoso flow for EMIR and PowerMos
- Only Quantus + Voltus-Fi flow accurate for FinFET designs!
- Integrated—execute Quantus solution under the hood from Voltus-Fi solution
- Self-Heating-Effect (SHE) support with Quantus and Voltus-Fi solutions
- Hierarchical EMIR support with Quantus QRC Extraction Solution only

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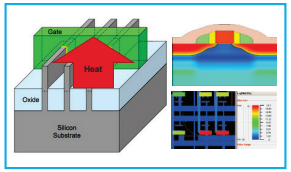
Self-Heating Effect (SHE) on TSMC FinFET Nodes

- What's SHE?
  - 3D transistor structure in FF has shorter gates and higher fins
  - Accumulated "heat" is "trapped" and hard to escape
  - Heat follows lowest thermal resistance path-vertically to interconnecting wire
  - Temperature on metal rises – impacting current density and EM



- TSMC's SHE - FEOL and BEOL Heating
  - FEOL: "Device heating"; thermal equations on RC given by encrypted TMI model
  - BEOL: "Interconnect heating"; equations based on RMS (Irms) current calculation
  - Final Twire is a function of FEOL and BEOL
  - TSMC's "5C rule" – adjusting FEOL layout to reduce T

Only Quantus QRC Extraction Solution + Voltus-Fi Power Integrity Solutions certified at TSMC to provide accurate SHE analysis!

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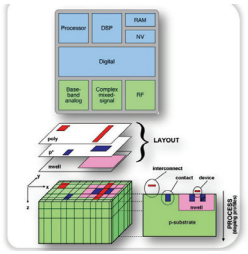
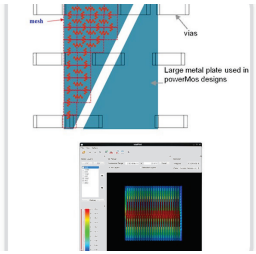
Market-Leading Features in Virtuoso Custom Design Platform



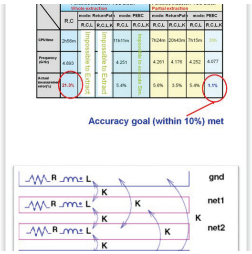
Substrate Noise Analysis

- Noise analysis between analog block-block or digital to analog block
- Full 3D substrate model; accurate within ≈7% of measurement data
- Provide isolation strategies (guardrings) to reduce noise in design



PowerMos Extraction

- Support automotive designs; high-voltage/current, wide-metal designs
- High accuracy Rdson
- Integrated flow in Virtuoso custom design platform with Voltus-Fi and Spectre/XPS solutions



Inductance Extraction

- Supports Partial Element Equivalent Circuit (PEEC), High-Frequency Effects, and Interconnect Fracturing
- Silicon Proven within 1.1% of measurement and Fast Henry
- Supports frequency points from DC to ≈100GHz with a single extraction run

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FinFET Designs are Getting Crowded and Complex

3D Problems Require 3D Solutions

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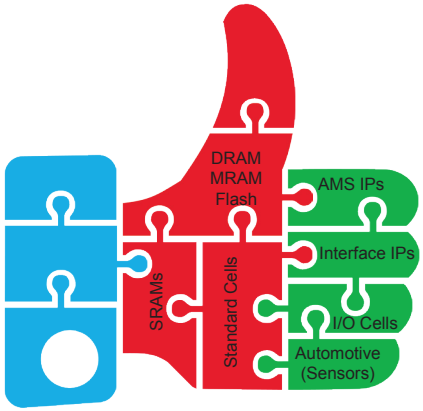
What Types of Designs MUST Use 3D Parasitic Extractor?



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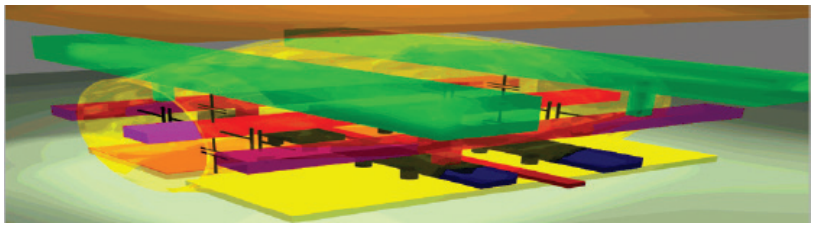
Quantus QRC Extraction Solution 3D Field Solver (FS)



Cloud-Ready and Massively Parallel

- Linear scalability to 1000s of CPUs
- Handle higher capacity
- Lowest memory consumption

Foundry-certified at TSMC to 7nm

- Best-in-class accuracy vs foundry golden data
- Certified at other foundries

Integrated in Quantus QRC Extraction Solution and other Cadence Tools

- Innovus Implementation System and Virtuoso custom design platform (including ADE)
- Virtuoso Liberate Characterization Solution
- Spectre APS and XPS Simulation

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